Reconfiguration of NPC Multilevel Inverters to Mitigate Short Circuit Faults Using Back-to-Back Switches

Weiqiang Chen, Ethan Hotchkiss, and Ali Bazzi

***Abstract*—The main focus of this paper is to propose a reconfiguration method to mitigate short circuit faults in a neutral point clamped multilevel inverter which is widely used as a power conversion system with distributed energy resources. Existing reconfiguration methods use either a redundant strategy or need a large number of additional devices pre-installed in the circuit; these will increase the bulk and complexity of the system. Most existing control-strategy-based methods distort the phase-to-neutral voltage, which results in degradation of power quality. To maintain control-strategy-based reconfiguration, avoid significant change to the circuit topology, and avoid phase voltage distortion, a new and practical reconfiguration method is proposed in this paper. The proposed method is applicable to neural point clamped (NPC) multilevel inverters at any voltage level and can mitigate short circuit faults in any device. A technique of switching series connected switches is selected to combine with the proposed reconfiguration method since it's a practical design consideration for realistic implementation. MATLAB/Simulink is used to simulate a five-level NPC inverter with non-idealities to verify the proposed reconfiguration method. A five-level NPC is also built and tested to experimentally verify the proposed method. Short circuit faults are injected to different devices and the proposed method is verified to quickly and effectively recover the NPC inverter from these faulty conditions.**

***Index Terms*—Fault tolerance, multilevel inverter, reconfiguration, short circuit fault.**

I. Introduction

SINCE many industrial applications require medium to high voltage, multilevel inverters (MLIs) have been widely usedin industry to sustain higher voltage stress due to their cascaded per-phase structure. Other advantages of MLIs include lower common-mode voltage, operation under both high and low switching frequencies, and lower total harmonic distortion (THD) [1]. MLIs have been widely utilized as power converters for distributed energy resources such as in wind energy systems [2], [3] and solar energy inverters [4], [5]. Due to the cascaded structure, more complex control strategies and more semiconductor devices are used in MLIs. The increased number of semiconductor devices increases the risk of failure since the failure of a single device could cause the whole inverter to fail. Researchers have studied the reliability of power electronics to a great extent in an attempt to reduce the risk of failure and to increase the reliability of power electronic systems for distributed energy resources[6], [7]. The most common faults that may occur in MLIs are open and short circuit faults in power switches [8]. One of the most common causes of semiconductor device degradation and failure is related to dielectric breakdown, which could cause the gate voltage to lose control over the collector current, causing a short circuit fault [9]. The short circuit circulation path could cause extra electric stress on other devices or a short circuit condition on the source side; this could result in severe damage to the inverter, source, and load when compared to open circuit faults. To avoid such damage, the redundancy provided by the increased number of semiconductor devices in MLIs is utilized by researchers to develop many effective methods to reconfigure MLIs to recover from faults.

The proposed reconfiguration method can effectively mitigate the most severe fault condition of semiconductors, i.e., short circuit fault. The proposed reconfiguration method can be activated by the trigger signal generated by any fault diagnosis or prognosis method. Compared to the existing reconfiguration methods, which utilize redundancy control strategies or add-on components, the proposed reconfiguration method has less additional components, and unlike some existing methods which also utilize less additional components, the proposed reconfiguration method maintains the peak value of output voltage in the reconfigured condition. The proposed reconfiguration method does not sacrifice the power quality of phase-to-neutral voltage or phase current, which typically occurs in the existing control-strategy-based reconfiguration methods. Further details on related literature and the advantages of the proposed method are shown in Section II. Also in Section II, more background is provided on neutral-point clamped (NPC) MLIs. Section III introduces the principle of the proposed reconfiguration method and a selected voltage balancing technique to achieve the synchronization of series-switched devices. Section IV shows simulation results to verify the proposed reconfiguration method. In Section V, experimental results of implementing the proposed reconfiguration method and the selected voltage balancing technique in a 5-level NPC inverter are shown. Section VI concludes the paper.

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II. Background

A. Post-Fault Reconfiguration Methods in MLIs

The NPC inverter was introduced 36 years ago [10], [11] and is the most widely used topology in industrial applications [12]. A 3-level example is shown in Fig. 1 for illustration. Therefore, many post-fault reconfiguration methods have been developed to ensure continuous operation of NPC inverters. NPC inverters can be switched by sinusoidal pulse width modulation (SPWM) or space vector modulation (SVM) [13]. In SVM, when device failure happens, some voltage vectors cannot be achieved, thus redundant vectors are utilized to compensate for the lost vectors [14], [15]. An effective way to tolerate device failure is to tie the phase which contains the failed component to the neutral point, change the control strategy and operate the two remaining healthy phases to achieve the balanced phase-to-phase voltage [16]-[21]. Another way is by changing the diodes D_1 to D_2 in Fig. 1 to controllable semiconductor devices and utilizing the flexible current path to tie the phase containing the failed component to the neutral point [22]. When the diodes are changed to controllable semiconductor devices, the NPC inverter is modified to become an active-NPC (ANPC) inverter. Redundancy is always a straightforward way to replace the failed device with a new one. This method has been used in other power electronic circuits [23], [24] and is a potential method for MLIs' recovery. Researchers have successfully achieved maintaining the inverter output waveform in fault-tolerant mode with a forth leg installed in the NPC inverter [25]-[28]. Even though the complexity is increased, the output waveform is effectively maintained after a failure occurs in one phase. A promising method in [29] has minor modification of the standard topology shown in Fig. 1; it utilizes fuses which are installed in series with the diodes D_1 and D_2 to disconnect diode legs, then the circulation of fault current is stopped when a short circuit happens.

Many effective reconfiguration methods for MLIs have also been achieved for different topologies. For MLIs which consist of cell units, such as cascaded H-bridge inverters, the failed cell can be bypassed, and the control scheme is modified to provide a balanced phase-to-phase voltage [30], [31]. To minimize the add-on components in a reconfigurable circuit, some control-strategy-based reconfiguration methods have been developed. Reconfiguration of carrier-based modulation strategy can effectively balance the phase-to-phase voltage after a failure occurs, and there are no additional components required in this method [32]. Due to the particularity of flying capacitor MLIs, a control-strategy-based reconfiguration method with minimum add-on component was proposed in [33], the same output voltage levels are achieved with subtraction of capacitor voltage in post-fault condition. For three-phase systems, when one device fails, the corresponding phase leg also fails and may cause unbalanced voltages and currents among phases; a neutral-shifted method was developed to handle the unbalanced condition [30], [34], [35]. These control-strategy-based reconfiguration methods are designed for different topologies and can reduce

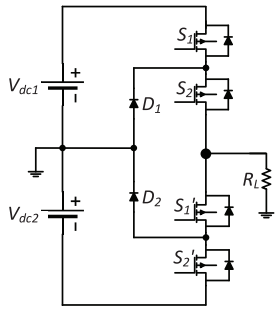


Fig. 1. Single Phase of a Three-level NPC.

the complexity and cost of MLIs significantly. More details of reconfiguration of MLIs can be found in [36].

Most of the existing reconfiguration methods for NPC have limitations: The SVM-based methods [9], [10] cause extra switching stress for the remaining healthy devices, and complexity of SVM-based methods increases dramatically with the level of MLIs. Tying the whole phase leg which contains only one failed device to the neutral point is not cost effective [16]-[21]. For example, if S_1 in Fig. 2 fails, the output of this phase leg is tied to V_3 to disable this phase leg even though the seven other devices are still in healthy condition; the inverter is thus operated with the remaining two phase legs to achieve a balanced phase-to-phase voltage. Also, after tying the failed leg to neutral, reduced peak value of the output voltage is observed. The ANPC with fault tolerance ability also has the problem of reduced peak output voltage and it is not applicable to various levels besides a 3-level ANPC inverter [22]. Redundant components [23], [24] and forth leg-based methods [25]-[28] are not cost effective since in MLIs, a large number of additional components is required. For the effective method in [29], complex circuitry and additional components are necessary to isolate the failed device or fault current circulation pass.

Existing methods for other topologies typically need additional devices installed in the power circuit even though they are not necessary for the original healthy operation: Additional switches or contactors are pre-installed in the circuit to disconnect the failed cell; these act as bypass contactors to bypass a failed cell or switch; for example, if an H-bridge cell in a cascaded MLI fails, a contactor is used to short the output sides of the failed cell to bypass it, which means that for each unit cell, a contactor should be installed [30], [31]. These cell-bypassing methods rely on the inverter topology, so they are not applicable to the widely-used NPC inverters. The method developed in [33] is only applicable to flying capacitor MLIs. While some control-strategy-based methods can be utilized in NPC inverters and do not require additional components, the reconfigured system typically has a distorted phase voltage and only phase-to-phase voltage is maintained; for example, if S_1 in Fig. 1 fails as an open circuit fault, V_{dc1} is lost in this phase, then the reference waveforms of the other two phases are modified accordingly to achieve the same phase-to-phase waveform [32]. This could cause significant degradation of voltage quality when phase voltage is of interest for grid-tied application, per-phase analysis, modeling, etc. Similar conditions of distorted phase-to-neu-

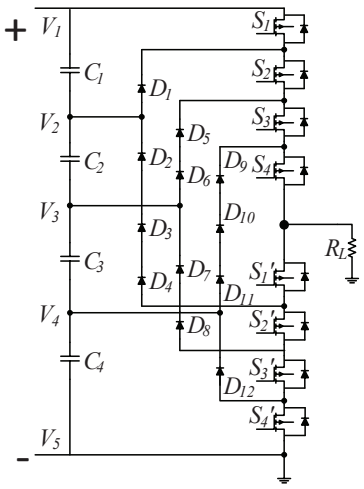


Fig. 2. Five-level NPC.

tral voltage happen with the neutral point shift (NPS) method [30], [34], [35].

Therefore, we propose a reconfiguration method that is applicable to mitigate short circuit faults in NPC inverters, and which provides simplicity, ease of implementation, and effectiveness while requiring minimal additional components. The proposed method is applicable to *any-level* NPC inverters, maintains the peak output voltage value, and retains balanced phase-to-neutral and phase-to-phase voltages and currents, simultaneously.

B. NPC MLI Background

The NPC inverter utilizes DC link capacitors to provide various voltage levels and uses proper switching actions of semiconductor devices to transmit the voltage levels to the load. The desired number of voltage levels determines the required number of semiconductor devices and DC link capacitors. Suppose the voltage level is N, then the number of semiconductor switched per leg is $2N$-2 and the number of DC link capacitors is N-1. The topology of a single phase five-level NPC is shown in Fig. 2, as this is the inverter topology used for simulation and experimental results in this paper. Level-shifted PWM is the control scheme used, where switching signals are generated by comparing a sine wave with four level-shifted sawtooth waves with same peak-to-peak values but different offsets [37]. The generation of level-shifted PWM for a five-level NPC is shown in Fig. 3. TABLE I summarizes the five-level operation. The generated PWM signals are sent to S_1 to S_4 in Fig. 2 and their conjugates are sent to S_1' to S_4', respectively.

III. Proposed Reconfiguration Method

A. Proposed Method

The proposed reconfiguration method utilizes the structure of the NPC inverter to reconfigure it from the original voltage level to a decreased voltage level. In this way, even though the number of voltage levels is decreased, the balanced conditions

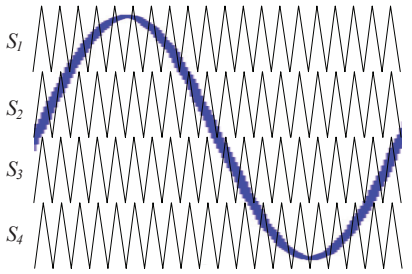


Fig. 3. Level shifted PWM for five-level NPC.

TABLE I
Five-Level Operation

S_1	S_2	S_3	S_4	Output Voltage
1	1	1	1	V_1
0	1	1	1	V_2
0	0	1	1	V_3
0	0	0	1	V_4
0	0	0	0	V_5

of both phase-to-phase and phase-to-neutral voltages are maintained. A five-level NPC inverter is used as an example to illustrate the proposed reconfiguration method. The proposed method requires installing a back-to-back switch pairs in the lines of different input voltage levels as shown in Fig. 3 where the back-to-back switch pairs are S_a-S_b, S_c-S_d, and S_e-S_f. It should be noted that the back-to-back switch pairs use semiconductors which allow for a fast transition from the failed condition to the decreased-level condition and limit any propagation of the fault current. However, these switches can also be replaced by contactors or relays if they can also provide a fast response. For example, if S_2 in Fig. 2 fails as short circuit fault, when S_3 and S_4 are in on-state, instead of transmitting V_3 to the load, a current from V_2 will flow to the load through D_1, S_2 to S_4. So, the back-to-back switches are used to stop the circulation pass of fault current from blocking the desired voltage.

In healthy condition, the switches S_a to S_f are turned on to ensure the transmission of different voltage levels. Suppose a short circuit fault happens to switch S_1 in Fig. 4(a) as shown in Fig. 4(b); the voltage level V_1 which is supposed to be blocked by S_1 will be passed through S_1, and as a result the diode D_1 will block the lower voltage level V_2. This causes a loss of voltage level V_2, which results in an unbalanced condition. Due to the symmetric configuration of the NPC inverter, the circuit is able to be reconfigured to a decreased level NPC inverter by switching S_1 and S_2, S_3 and S_4, S_1' and S_2', S_3' and S_4' in four pairs which are highlighted by four green dotted rectangular boxes as shown in Fig. 4(c), and turning off S_a, S_b, S_e and S_f as shown in Fig. 4(d). In Fig. 4(d), D_1 to D_4, and D_9 to D_{12} are also disabled with turning off S_a, S_b, S_e and S_f. The disabled components are marked as gray, and the equivalent circuit in reconfigured condition is also shown in Fig. 4(d). The three-level operation in a five-level NPC inverter is listed in TABLE II. As with other reconfiguration methods, the trigger signal of back-to-back switches should be from a fault diagnosis or prognosis algorithm which is used

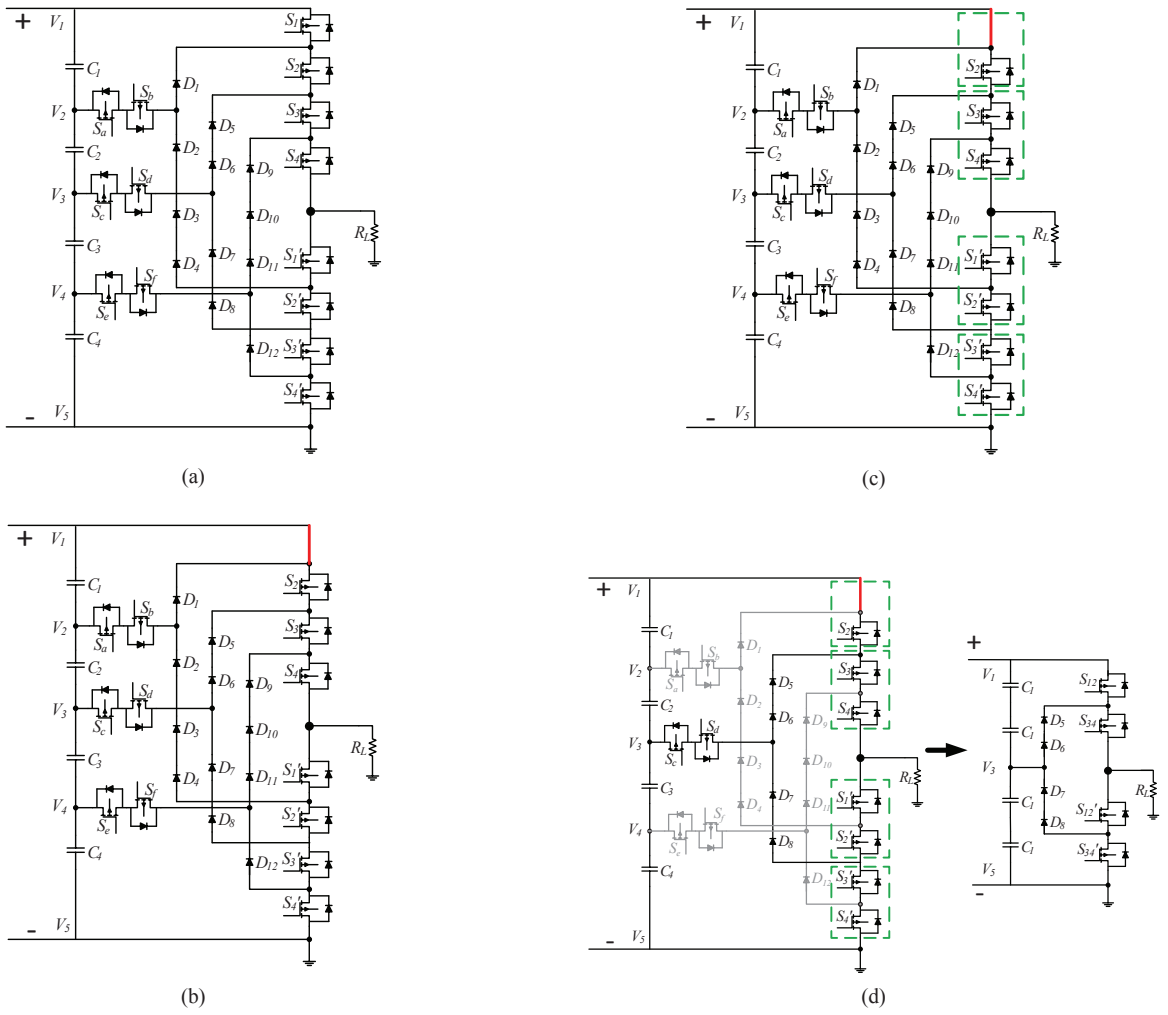


Fig. 4. Proposed topology (a) Healthy condition, (b) Short circuit fault in S_1, (c) Switching in pairs, (d) Fully reconfigured condition with turning off back-to-back switches S_a, S_b, S_e and S_f.

TABLE II
THREE LEVEL OPERATION IN A FIVE-LEVEL NPC

S_1	S_2	S_3	S_4	Output Voltage
1	1	0	0	V_1
0	0	1	1	V_3
0	0	0	0	V_5

to initiate the reconfiguration process. For example, diagnosis methods that have been explored by the authors and which complement this work are shown in [38]. Therefore, the shorted condition of any switch can be considered a passthrough since switches can be paired to tolerate the short circuit condition, and the short circuit path to the source is eliminated by the back-to-back switches.

Even though the voltage level is decreased, the unbalanced condition caused by the short circuit fault is resolved with very limited additional components. The redundancy strategy and forth leg methods can maintain the same voltage level in the post-reconfigured condition [25]-[28], but many more additional components and complicated control strategies are necessary when compared to the proposed method. The ANPC can achieve balanced phase-to-phase voltage without additional components, but it disables the remaining healthy components in the failed leg which is not cost effective. The peak value of output voltage is also reduced significantly [22]. The NPS method achieves a decreased level condition in the failed phase leg without any additional components [30], [34], [35]. However, it also reduces the RMS value of the phase voltage and it is more applicable to open circuit faults of MLIs that contain unit cells. The number of the back-to-back switches is determined by the voltage level of the NPC inverter, if the original voltage level is N, then the required number of back-to-back switches is N-2. This applies to both single-phase, three-phase, or higher phase NPC inverters since the back-to-back switch pairs are shared by all phases. With the N-2 back-to-back switches, the N-level NPC can be reconfigured to different voltage levels.

Suppose that the reduced voltage level is M; if (N-1)/(M-1) is an integer, then an N-level NPC inverter can be reconfigured to M level NPC inverter. The achievable voltage levels of different Llevel NPC inverter are summarized in TABLE III. A drawback of the proposed reconfiguration method is that the sustained

TABLE III
SUMMARY OF ACHIEVABLE VOLTAGE LEVELS

Original Voltage Level	Reduced Voltage Level
3	2
4	2
5	3 & 2
6	2
7	4 & 3 & 2
8	2
9	5 & 3 & 2
…	…

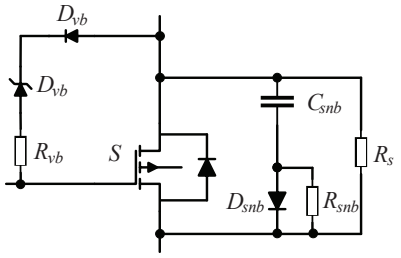


Fig. 5. Hybrid voltage balancing circuit.

voltage of the semiconductor which is in pair with the failed semiconductor is doubled, so the used semiconductor should have higher voltage rating.

B. Synchronization of Series-Switched Devices

The proposed reconfiguration method requires switching series-connected devices, so voltage balancing problems should be considered. When there is a difference in turn-on and turn-off switching times among devices, the voltage of each device will be different, which causes extra voltage stress on some devices [39]. Unbalanced voltage sharing can also be caused by spread of device dynamic and static parameters [40]. To resolve this issue, a proper voltage balancing technique for series-connected semiconductors is chosen. Two main considerations are 1) The voltage balancing technique should use a separate gate driving circuit for each device since one driving circuit for several semiconductors is not applicable to the original healthy operation (an example technique that is not applicable here is shown in [41]); 2) The voltage balancing technique should not have the components which are not necessary for the original healthy operation. Taking both considerations into account, a hybrid voltage balancing method for series-connected semiconductors in [40] is chosen. This method has not been implemented in MLIs but in this paper, it is successfully implemented in an NPC inverter and contributes to balance the voltage of the series-switched devices. The hybrid technique consists of an active voltage clamping circuit and a passive snubber circuit. The circuit for the hybrid technique is shown in Fig. 5, and each semiconductor will be modified as such. Even though the voltage clamping circuit and snubber circuit are added into each switch, they are not only helpful for synchronizing and balancing series-connected switches, but also improve the performance of original healthy operation such that when more than two switches are off, the sustained voltage of each switch is balanced.

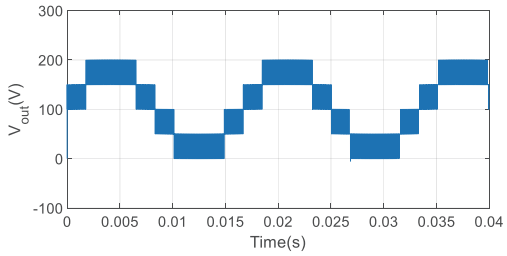


Fig. 6. Output waveform of healthy condition.

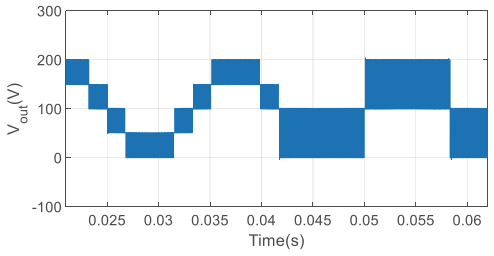


Fig. 7. Output waveform of transmitting healthy condition to reconfigured condition.

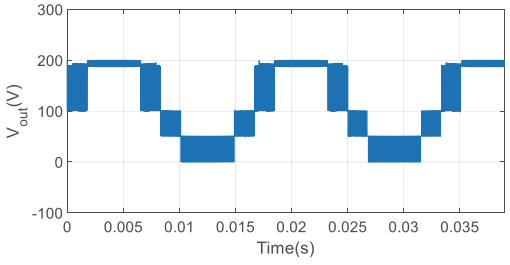


Fig. 8. Output waveform of S_1 short circuit fault.

IV. SIMULATION RESULTS

Simulation in MATLAB/Simulink are first performed to verify the proposed reconfiguration method. A five-level NPC with the same topology as Fig. 1 is built and the switching scheme is level-shifted PWM. For illustration purposes, the DC bus voltage is 200 V, switching frequency is 10 kHz, and fundamental frequency is 60 Hz. The healthy five-level operation output voltage waveform is shown in Fig. 6. Note that the voltages have a DC offset since the reference point is chosen at the negative DC bus side as shown in Fig. 1.

The proposed reconfiguration method is implemented when the circuit is in healthy state; the transition from healthy condition to reconfigured condition is shown in Fig. 7. The distorted phase-to-neutral output waveforms caused by short circuit fault on S_1 and S_3 are shown in Fig. 8 and Fig. 9, respectively. The proposed reconfiguration method is thus implemented when the short circuit in S_1 and S_3 is mitigated using the proposed method as shown in Fig. 10 and Fig. 11, respectively. In Fig. 10 and Fig. 11, the short circuit had occurred before the shown

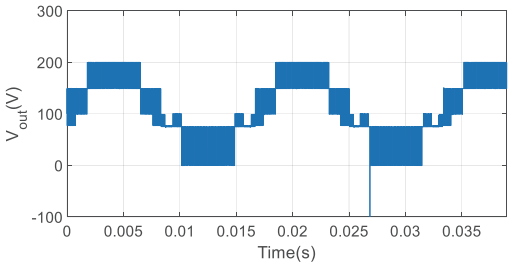


Fig. 9. Output waveform of S_3 short circuit fault.

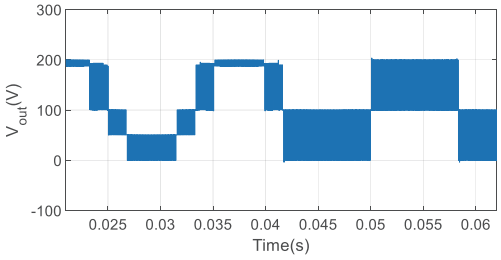


Fig. 10. Output waveform of transmitting S_1 short circuit condition to reconfigured condition.

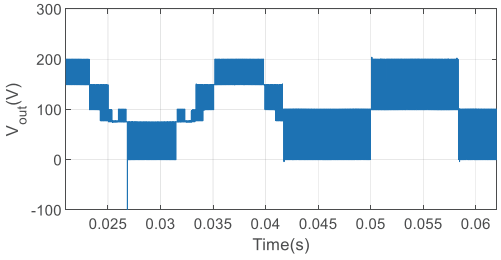


Fig. 11. Output waveform of transmitting S_3 short circuit condition to reconfigured condition.

time scale, and the reconfiguration method is engaged at 42 ms. Results show that the proposed method can be successfully implemented while the circuit is in healthy or failed conditions and indicates that the proposed method can be integrated with either fault diagnosis methods or fault prognosis methods before a fault occurs. The proposed method can clearly balance phase-to-neutral voltages while requiring minimal circuit modification. Experimental verification will also illustrate the voltage balancing and switch synchronization, which is not required but an added benefit to the proposed method.

V. Experimental Verification

A. Experimental Results of a Five-Level NPC Inverter

A five-level NPC inverter which has the same topology as Fig. 1 has been built in hardware. The four isolated DC supplies are shown in Fig. 12 to eliminate the voltage balancing need across capacitors. The whole setup is shown in Fig. 13, with one phase of the inverter used for demonstration purposes. LabView software is used to generate the level-shifted PWM signals and communicate with gate driver board through NI FPGA. The

Fig. 12. Isolated power supplies.

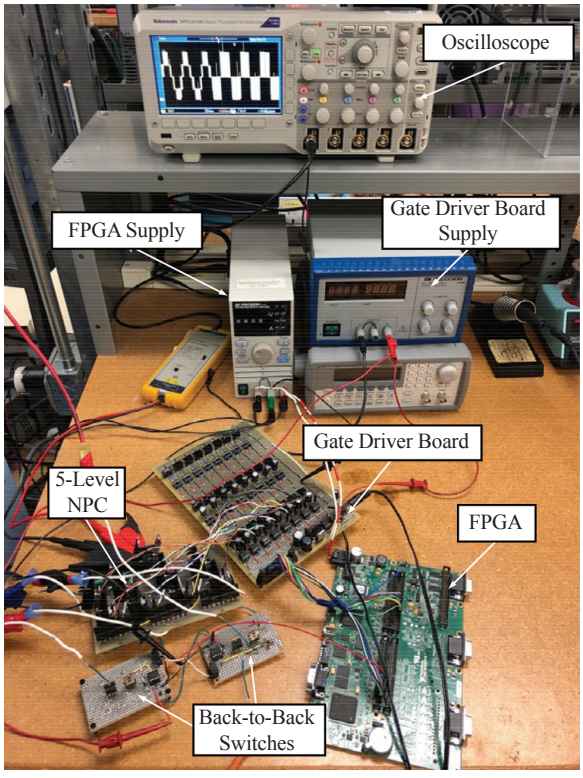


Fig. 13. Hardware Setup.

platform performs well in healthy condition with 200 V DC bus and 200 Ω load as shown in Fig. 14. A low voltage condition of 60 V is used when implementing the proposed reconfiguration method to limit the short circuit energy during test; a transient of implementing the proposed method in healthy condition is shown in Fig. 15.

The first step in verifying the proposed method is to ensure that synchronous switching and voltage balancing across series devices is achieved. For this purpose, the hybrid voltage balancing technique in [40] is implemented in the five-level NPC inverter. Fig. 16 shows the experimental results of the unbalanced condition of S_1 and S_2 drain-to-source voltages without the hybrid voltage balancing technique. Fig. 17 shows the balanced

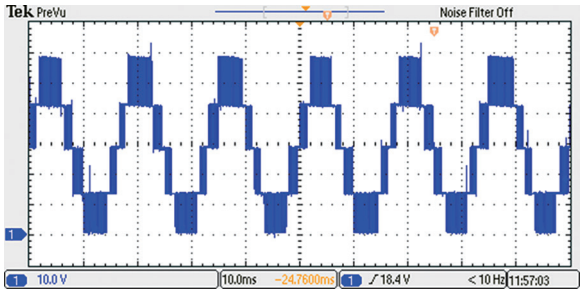


Fig. 14. Healthy operation with 200 V DC bus (10 V/div, 10 ms/div).

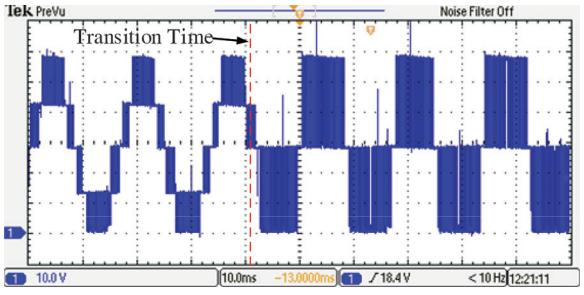


Fig. 15. Phase-to-neutral voltage when implementing proposed reconfiguration method in healthy condition (10 V/div, 10 ms/div).

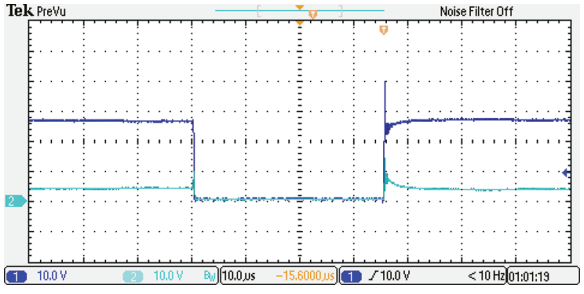


Fig. 16. Unbalanced condition of S_1 and S_2 voltage (10 V/div, 10 µs/div).

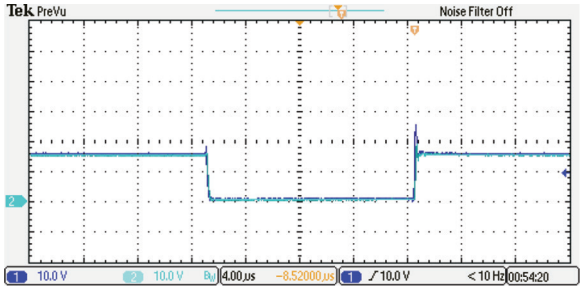


Fig. 17. Balanced condition of S_1 and S_2 voltage (10 V/div, 4 µs/div).

condition of S_1 and S_2 drain-to-source voltages with the hybrid voltage balancing technique. Fig. 16 and Fig.17 verify the effectiveness of the synchronization and hybrid voltage balancing technique in the NPC inverter, and ensures that the proposed method is now applicable.

For validation purpose, the five-level NPC inverter is reconfigured to a three-level when a short circuit fault happens, and only S_a, S_b, S_e, S_f from Fig. 4(a) are actually installed to stop

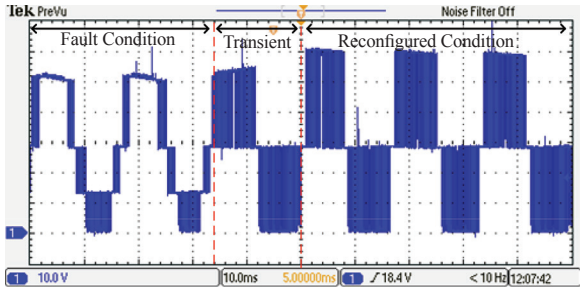


Fig. 18. Phase-to-neutral voltage when implementing proposed reconfiguration method in S_1 short circuit fault (10 V/div, 10 ms/div).

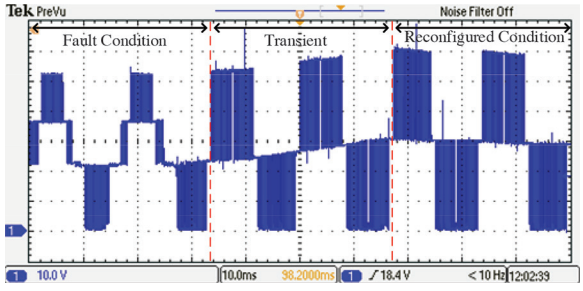


Fig. 19. Phase-to-neutral voltage when implementing proposed reconfiguration method in S_3 short circuit fault (10 V/div, 10 ms/div).

the fault current path. The proposed reconfiguration method is implemented when the short circuit fault happens to S_1 or S_3. Fig. 18 shows the transient of implementing the proposed reconfiguration method when S_1 fails as a short circuit, Fig. 19 shows the transient of implementing the proposed reconfiguration method when S_3 fails as short circuit. In both Figures, the short circuit fault had occurred before the first two cycles shown, and at the beginning of the third cycle, the proposed method is engaged. Waveform deflection is observed during the transient period, which may be due to parasitic elements and/or signal propagation delay. These result in unsynchronized turning off the back-to-back switches while changing control of semiconductor devices to pairs. After the short transient period, the MLI is reconfigured to the decreased-level condition. The method is shown to successfully maintain symmetry in the phase-to-neutral voltage after being distorted by the short-circuit fault. Therefore, the proposed reconfiguration method successfully reconfigures the failed inverter in a fraction of a fundamental cycle. The inverter can then maintain load support and operate in a decreased level condition with balanced phase-to-neutral voltage unlike other existing methods and maintains balanced drain-to-source voltages across series switches as needed.

B. Summary: Comparing the Proposed Method with State-of-the-art

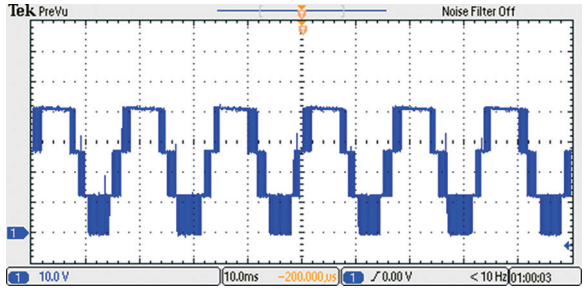
To summarize the state-of-the-art of the proposed reconfiguration method, the shortages of existing reconfiguration methods are checked first. The SVM-based method [14], [15] has more complex control in the reconfigured condition, and utilizing the redundant vector means more switching actions are assigned to the remaining healthy devices which causes extra stress on

TABLE IV
COMPARISON OF DRAWBACK OF PROPOSED METHOD AND EXISTING METHODS

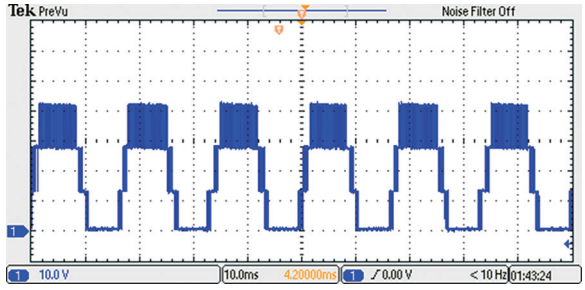
	Proposed Method	*SVM*	*IFPL*	*ANPC*	*CLR*	*FLB*	*FUI*	*FCI*	*FCV*	*MRS*	*NPS*
Reduced Peak Value			●	●						●	●
Unbalanced Per-phase Condition			●	●						●	●
Excessive Add-on Components					●	●	●	●			
Excessive Complexity of Control		●		●			●				
Extra Stress on Devices	●	●					●	●			
Not Applicable to NPC Inverters								●	●		
Not Applicable to Different Levels				●							

these devices. The method of isolating a faulty phase leg (IFPL) [16]-[21] has the drawbacks of reduced output voltage peak and unbalanced per-phase voltages, since the MLI is operated with only two phases. The ANPC fault-tolerant inverter [22] has the same drawbacks of IFPL and since it has additional switching devices, the control complexity is increased. This ANPC fault tolerant inverter is only applicable to a 3-level condition, which means that it is not applicable to the MLIs with other voltage levels. The component-level redundancy (CLR) strategy [23], [24] is not feasible for MLIs since the number of semiconductor devices is very large. The forth-leg-based (FLB) method [25]-[28] has a redundant phase leg, which is not cost effective. The method of utilizing fuses to isolate a faulty device (FUI) [29] has many of add-on components, complex control and extra stress on the remaining healthy devices. The faulty cell isolation method [30], [31] requires additional components installed in each unit cell which is not cost effective, and remaining healthy devices in reconfigured condition will have more voltage stress; also, since this method is only applicable to MLIs which contain unit cells, it is not applicable to NPC inverters. The method of utilizing different voltages of flying capacitors (FCV) [33] is only applicable to flying capacitor MLIs. The method of modifying the reference signal (MRS) [32] does not require add-on components and is easy to achieve, but it causes reduced output voltage peak and unbalanced per-phase condition. The NPS method [30], [34], [35] also has the drawback of reduced output voltage peak.

TABLE IV summarizes the drawbacks of the existing reconfiguration methods and compares these methods with the proposed method. Most of the existing methods have more than two drawbacks, and even though the CLR and FLB only have one drawback, the excessive add-on components significantly increase the system cost. Also, FCV is not applicable to NPC inverters. CLR, FLB, FUI and FCI require add-on components where the number of components increases with the increased voltage levels and if it is a three-phase system, the required number of components is tripled. However, the number of additional components per phase in the proposed method is less than any of these four methods and is not affected by the number of phases, which reduces the total number of additional components significantly. The only drawback of the proposed method is extra voltage stress on the remaining healthy devices in reconfigured condition, which also appears in some of the existing reconfiguration methods.



(a)



(b)

Fig. 20. Phase-to-neutral voltage when implementing MRS method (a) ALM (b) 120° DPWMMIN (10 V/div, 10 ms/div).

Among the existing reconfiguration methods, MRS and NPS are control-strategy-based methods, which do not require additional components and are easy to achieve. These two methods gain the most interest to compare with the proposed method. The decreased peak value of output voltage is an issue when the load requires a stable voltage level. The distorted per-phase waveform is as issue in the following conditions: 1) per-phase analysis of Y-connected loads, 2) unbalanced load conditions with neutral current flow, 3) grid-interconnection standards that limit the line-to-line voltage maximum (e.g. IEEE1547 and AS4777). To better understand the output voltage distortion using both MRS and NPS methods, the phase-to-neutral waveforms of these two methods are generated experimentally and are shown in Fig. 20 and Fig. 21, respectively. It should be noted that both the amplitude-limited modulation (ALM) and 120° discontinuous pulse width modulation minimum (DPWMMIN) modulation methods shown in Fig. 20 as subcategories of the

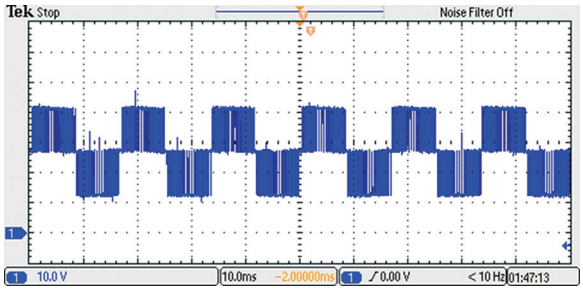


Fig. 21. Phase-to-neutral voltage when implementing NPS method (10 V/div, 10 ms/div).

MRS method. From the figures, it can be observed that the peak value of the per-phase voltage is reduced significantly, and unbalanced condition happens. The NPS method seems to have a balanced phase-to-neutral voltage waveform, but the voltage waveforms of the other two phases remain the same, which causes an unbalanced condition between the three phases.

VI. Conclusion and Future Work

A practical reconfiguration method for short circuit faults in NPC MLIs is proposed in this paper, which overcomes several weaknesses of existing reconfiguration methods. The proposed reconfiguration method is applicable to any NPC MLI with any number of voltage levels and can mitigate short circuit faults on any device. Simulations are shown to verify the effectiveness of the proposed reconfiguration method. A hybrid voltage balancing technique is selected and implemented to enhance the performance of the proposed reconfiguration method. A single-phase hardware platform is built and tested in healthy condition and reconfigured condition to demonstrate the effectiveness of the proposed method in mitigating short circuit faults. Future work focuses on achieving the proposed reconfiguration method at higher power and augmenting a fault diagnosis method to engage the proposed method.

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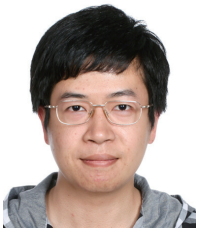

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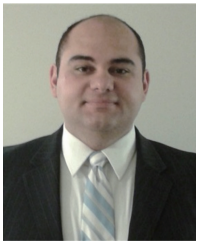

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